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**Blatt 2 der Bescheinigung
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Boundary Scan Delay Chain for Cross-Chip Delay MeasurementDescription

5 The invention relates to a method for achieving delay measurement functionality, to a boundary scan cell, an integrated circuit and an electrical device each having delay measurement functionality and to a method for performing delay measurement.

10 As known for a person skilled in the art, usually the design of complex ASICs (Application Specific Integrated Circuits), SOCs (System On Chip) and/or ICs (Integrated Circuits) in time with required quality levels is a major challenge. Based 15 thereon it is often very important for ASICs/SOCs/ICs, in the following description generally referred-to as integrated circuit, to have an easy accessible delay measurement path for several reasons. The delay of a long path running across the whole integrated circuit (cross-chip) of an electrical 20 device through lots of instances, such as inverters and/or multiplexer makes it possible to measure final process parameters of the integrated circuit within a best case and worst case production process window.

25 Usually, this information is very important for the production testing at the vendor side. But very often this information also is necessary at the circuit pack or PCB (printed circuit board) level, system test level and/or even

in the field, for example in case of problems occurred in functionality, timing and/or debugging, the "quality level" reached by the integrated circuit should be determined.

Additionally, even for the characterization of the delay.

5 modeling during different design phases, such as estimation, floor planning, trial and/or final layout a dedicated delay path may help in qualifying the delay models together with the topological information of the database.

10 Thus, especially for a quality ranking of an electrical device, a design flow and/or a vendor dealing with complex integrated circuits it is very important to know how accurate the timing modeling fits with the real devices to estimate the timing margin between simulation models and their

15 corresponding real devices. As mentioned above, in case of device problems it is important to know the relative device performance within the best case to worst case process variations. The process quality level can be determined, if a delay measured on an integrated circuit sample can be

20 compared with the delay calculated by a timing simulation or by STA (static timing analysis) with certain process quality assumptions.

At present, a method for determining a quality level of a 25 complex integrated circuit is involving a simple delay strobing on the (production) tester, which only indicates a passing or failing result but does not give an exact delay value. A further approach comprises the definition of a more or less random delay path within the design resulting in an 30 ad hoc and none-standard solution concerning the topology, implementation, access and initialization.

Further known solutions for delay measurement and process characterization involve the use of a so called NAND-tree and/or a PROCMON-cell, i.e. a process-monitor-cell, both requiring additional instances, needing some efforts for 5 implementation, initialization and/or access and might be vendor dependent as disclosed for example by LSI Logic, "Design Manual and Procmon Application Note" or Texas Instruments, "GS30 Design Manual and TDL Documentation", the contents of which are incorporated herein by reference.

10

An object of the invention is to provide a new and improved approach for delay measurement of an integrated circuit that is substantially independent of vendors, technology and/or used development tools with a minimum of implementation 15 effort in design time and gate resources.

Further objects are to provide a delay measurement functionality which can be produced at low costs and may cover a long path across an integrated circuit and with an 20 easy access and initialization for performing the delay measurement without the need of a complicated and/or expensive IC-tester.

The inventive solution of the object is achieved by methods 25 incorporating the features of claim 1 or claim 18, by a boundary scan cell incorporating the features of claim 8 and by an integrated circuit and device comprising the features of claim 12 or 17. Advantageous and/or preferred refinements and/or developments are the subject matter of the respective 30 dependent claims.

According to the invention it is proposed to provide at least one boundary scan cell, each having a storage layer between a

scan input port and a scan output port constructed to be used within a scan chain of an integrated circuit for boundary scan testability, to analyze each of the boundary scan cells to identify a redundant state which is used to extend the 5 scan cell by creating an additional local path between the respective scan input and scan output ports bypassing the respective storage layer and to implement each scan cell in the integrated circuit by creating said scan chain.

10 One of the advantages of the present invention is, that by means of said local bypass path the scan input port and the scan output port are connected in a purely combinational manner for performing a delay chain that may include all input, output and bi-directional boundary scan cells.

15 Moreover due to the fact that a redundant state is used for providing delay measurement functionality the inventive approach is still conform with the original boundary scan testability requirements.

20 By using a boundary scan cell for delay measurement having a functional layer and a storage layer which is bypassed for delay measurement no additional ports and/or test signals are necessary for the boundary scan cells used within the 25 inventive boundary scan cell delay chain. Since furthermore no additional design instances and connectivity are necessary because only commercial or user library elements are modified internally and the cell ports are still the same, the implementation effort in design time and gate resources is 30 minimal and substantially independent of vendors, technology and used development tools.

To obtain a relatively long delay chain for measuring to reduce the influence of fixed measuring errors and to preferably spread the delay chain across the whole chip to cover several process variances of the device, it is 5 suggested to use so called boundary scan cells substantially avoiding any additional topological impact because only the boundary scan cells have to be placed and routed according the boundary scan and functional requirements. Since it is in general mandatory to use such boundary scan cells for a 10 boundary scan chain in complex ASICs, SOCs and/or ICs, the delay chain, as an advantageously consequence, is implemented automatically.

According to a very preferred embodiment it is proposed to 15 use boundary scan cells according to the IEEE Standard 1149.1, i.e. a standard methodology for interconnect testing on PCB, or to a standard derived from the IEEE Standard 1149.1.

20 Furthermore, according to a further preferred embodiment, it is proposed to connect the local bypass path and the storage layer of a respective scan cell with the scan output port via a multiplexer which is controlled by the shift signal from a given test access port controller to add a delay between the 25 shift registers for increasing the hold time margin, i.e. to provide a skew safety margin for the test clock (TCK).

The local bypass path may comprise additional library elements for further delay or level adjusting, such as 30 inversions.

Moreover, since in substantial no additional test ports and/or signals are necessary, an easier initialization and

simulation setup as well as a delay measurement without a usual complex ASIC/IC tester even on board is guaranteed. Based thereon the preferred method of performing delay measurement of an integrated circuit or electrical device 5 having an integrated circuit with an inventive delay chain merely comprises the entering of the delay measurement mode preferably by setting the boundary scan TAP-controller in a test-logic-reset-state (TRSTN =0) and by applying a data transition on the test data input (TDI). The delay 10 measurement itself can be performed at the given test data output path (BSR_TDO) for the scan testability.

Depending on specific device architectures, an additional delay chain output port (DCO) connected with the test data 15 output path (BSR_TDO) may be provided.

Even if boundary scan cells usually consist of different logic cells for different vendors and/or technologies there are no special logic cells required. Thus by modifying such 20 scan cells according to the inventive approach a delay chain is ensured, which is in contrast to prior vendor specific delay chains substantially vendor and technology independent and is moreover still including boundary scan test compatibility. Since the inventive delay chain can be 25 accessed by setting two test pins or ports to a certain value, wherein such test pins are pre-given, easily accessible on PCB due to IEEE 1149.1 requirements and/or can be shared with other test pins, no additional pins are required.

30

Thus, the inventive approach results in a new and improved standard methodology addressing the issues of delay measurement and „quality level“ determination for integrated

circuits, in general.

Subsequently the invention is described in more detail, in particular on the bases of a very preferred embodiment and 5 with reference to the attached drawings, in which:

Fig. 1 is a schematic diagram of a preferred boundary scan cell modified according to the invention,

10 Fig. 2 is a schematic diagram of a standardized boundary scan cell prior to the modification according to Fig.1,

15 Fig. 3 schematically depicts a chip having a boundary scan delay chain formed by serially connected scan cells according to Fig. 1, and

20 Fig. 4 is schematically depicting an inventively modified boundary scan delay chain architecture based on boundary scan cells according to the IEEE Standard 1149.1.

25 For the following description and for the attached set of claims complex ASICs, SOCs and ICs are generally referred-to as integrated circuit. As known by a person skilled in the art, ordinary scan cells connected to form shift registers are often incorporated or implemented in integrated circuits for scan testability reasons.

30 Based thereon, reference is made to Fig. 1 and 2 schematically showing a boundary scan cell having delay measurement functionality according to the invention and the standardized boundary scan cell according to the prior art

without that functionality, respectively. However, for a better understanding of the preferred exemplary refinement of the invention based on a boundary scan cell (Fig. 2) according to IEEE Standard 1149.1 reference is made to IEEE 5 Standard 1149.1 - 1990, "Test Access Port and Boundary-Scan Architecture", the content of which is entirely incorporated to the disclosure of the present invention by reference.

As can be seen from Fig. 1 and 2 the boundary scan cell is 10 connected between functional paths, such as between input buffers to core or between core to output buffers by a parallel input port PI and a parallel output port PO. In normal mode, i.e. in functional mode, the input port PI is directly connected to the output port PO by setting the mode 15 signal to "0".

Between a scan input port SI and an scan output port SO a storage layer is integrated to form shift registers by serially connecting the scan output port SO with the scan 20 input port SI of a further scan cell to generate a scan chain as it is exemplary depicted in Fig. 3 showing a chip having such a boundary scan chain. The control signals for shift, capture and hold functionality as well as the mode signal are generated by a test access port (TAP) controller, based on 25 the preferred embodiment according to the IEEE Standard 1149.1.

Referring to the prior art according to Fig. 2, the information at the scan output port SO is of interest only in 30 the shift mode and hence, the output SO is equal to Q. However, as can be seen from Fig. 2 showing the known ordinary boundary scan cell, in all other cases, i.e. if shift is set to "0" to be inactive, the output port SO is

totally redundant.

According to the inventive approach as depicted in Fig. 1 this redundant status of the ordinary boundary scan cell is 5 used to create an additional combinational delay path between the input port SI and the output port SO.

For realizing such additional combinational delay path the storage layer between the input and output ports SI and SO is 10 bypassed by the inventive local path BP.

According to the preferred but exemplar embodiment of Fig. 1, the additional local bypass BP and the storage layer are connected via an additional multiplexer MUX which is also 15 controlled by the shift signal from the TAP-controller.

Consequently and based on that improvement, a delay mode can be entered by setting the shift mode as being inactive, i.e. shift is set to "0". During this delay mode the scan output port SO is not redundant but in functional dependence on the 20 input port SI, i.e. $SO = f(SI)$.

Moreover, by setting the shift mode to be active to obtain at the scan output port SO the information Q, i.e. if shift mode = "1", then $SO = Q$ and the original scan mode functionality 25 additionally may be used.

As mentioned above, by connecting a plurality of scan cells serially to form a shift register, a scan chain according to Fig. 3 is created. Thus, by using an amount of the inventive 30 modified scan cells (Fig. 1) to form such a scan chain with the input port SI of the first scan cell connected to a test data input TDI preferably providing the stimuli input for boundary scan testability and the output port SO of the scan

cell forming the end of the scan chain to a test data output TDO an additional delay chain is automatically created from the test data input TDI to the end of the boundary scan register BSR, such as to BSR_TDO (Fig. 4). Based on the 5 exemplar refinement using a boundary scan cell according to the IEEE Standard 1149.1 a delay chain is performed at least from TDI to BSR_TDO, as can be seen from Fig. 4 depicting the specific boundary scan delay chain architecture according to the preferred embodiment.

10

Thus, by use of existing, usually standardized boundary scan cells and by creating a purely combinational delay path all input, output and/or bi-directional boundary scan cells may be included in the delay chain, wherein no additional ports 15 or test signals are necessary for the modified delay chain cells. Furthermore, since merely scan library elements are modified internally and the cells have to be routed and placed according to the scan and functional requirements no additional design instances, connectivity and/or topological 20 impact are necessary for creating that inventive scan delay chain in a standardized manner.

Moreover, by using boundary scan cells, a delay chain running across a whole integrated circuit, such as on a chip 25 according to Fig. 3, can be achieved to cover several process variances of the device comprising that integrated circuit or chip for performing a so-called cross-chip delay measurement incorporating a plurality of nodes, elements, layers and/or vias.

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Based thereon, a delay between the test data input TDI passing the boundary scan register BSR to the BSR_TDO-path, according to the highlighted delay measurement path of Fig.

4, is in functional dependence on the number of pins, i.e. substantially of the number of boundary scan cells incorporated, on the multiplexers, inverters and/or other delay or library elements embedded in the improved scan 5 cells, on cross-chip interconnections, buffers, capacitive loads, on the process, the temperature and/or on the power supply variations.

As can be seen in Fig. 1, the inventive local bypass path BP 10 can further comprise library elements 10 for additionally connecting respective delay elements. In any case, however, no additional design instances and connectivity are necessary, since only given scan library elements are modified internally and the cell ports are still the same 15 within the modified delay scan cell. Furthermore, since the improved scan cells merely have to be routed and placed according to the usually standardized scan and functional requirements, a delay chain including the improved boundary scan cells is still conform to the boundary scan 20 functionality requirements, i.e. with regard to the exemplary embodiment to the IEEE Standard 1149.1.

Moreover, the additional multiplexer MUX within the local bypass path BP is advantageously adding a delay between the 25 shift registers which increases the hold time margin, i.e. to improve the skew safety margin for the test clock TCK for avoiding skew and/or holding-time problems.

Mainly referring next to Fig. 4, the principle delay chain 30 access and initialization mechanism based on the preferred embodiment, i.e. based on the IEEE Standard 1149.1, is described in more detail. To get into the boundary scan delay chain mode it is necessary to find a state within the test

access port controller (TAP) where the shift control is not active. This, however, is the case in the test-logic-reset state which is (asynchronously) entered when the reset pin TRSTN is set to "0". As a consequence, the path from the 5 boundary scan register BSR comprising the serially connected boundary scan cells to the test data output pin TDO, i.e. in particular to the path BSR_TDO, is in functional dependence on the test data input TDI for providing the test stimuli input.

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However, based on the example using a boundary scan cell chain according to the IEEE Standard 1149.1 the delay path or chain is still not accessible from the device pin. According to that standard an other part or register, such as a bypass 15 register BR, may be automatically selected and not the boundary scan register BSR. Furthermore, also a multiplexer BS-MUX and a test data output flip-flop TDO-FF acts as blocking elements for the inventive boundary scan delay chain. Thus, according to a preferred refinement to still 20 keep the access and initialization simple, the BSR_TDO-path is bypassing the multiplexer BS-MUX and the output flip-flop TDO-FF to a separate delay chain output test pin DCO.

It has to be noted, however, that there are no compelling 25 reasons in general, to provide a delay test pin DCO separated from a given test data output pin TDO, as it is obvious for a person skilled in the art.

The separate test pin DCO can be controlled by a separate 30 test mode signal TM to keep it in tristate condition during functional mode. But even this is optional, since the test data input pin TDI is pulled to operating voltage V_{DD} according to the standard, i.e. TDI = "1" and hence, keeps

the whole boundary scan delay chain path quiescent in functional mode. As mentioned above with regard to the test pin DCO also the pin TM may be shared with other test pins, such as a test pin for a RAM (random access memory) test. 5 mode, a PLL (phase locked loop) test mode, a core scan test mode and/or similar test modes.

Consequently, for performing a delay measurement, in particular a cross-chip delay measurement an easy and direct 10 access by a given test data input TDI and test data output TDO or delay chain output DCO is provided when using inventively modified boundary scan cells. Also, the quality level of a device can easily be determined on a circuit pack 15 without any need of additional IC-testers or special loadboards.

For an implementation of the inventive scan delay chain the following flow preferably may be used. Prior to create a respective (boundary) scan-chain according to given scan and 20 functionality requirements by means of specific favorite tools, the standard boundary scan cells have to be extended into the inventive boundary scan delay chain-cells according to the afore-discussed inventive approach. During the logic synthesis of the scan-chain, the boundary scan delay chain 25 path is defined as being a false path to avoid futile optimization efforts. Subsequent to the performing of simulation to verify a correct standardized scan behavior, a static timing analysis (STA) as known should be performed on the respective delay chain output-port DCO for an estimated, 30 floorplan and/or layout timing. Based on that timing information an estimation of the accuracy of wiring and/or load models and the definition of a process window, i.e. the best and worst case production process window can be carried

out.

According to the practical use of the inventive scan delay chain measurement providing a substantially standardized.

5 methodology, there are basically three different fields of applications, i.e. during the design, the production of an electrical device comprising complex integrated circuits and in the field itself.

10 In detail, one of the preferred applications is the delay characterization during the design implementation process with link to layout. Starting from a top-level assembly, an estimated (wiring) delay calculation and static timing analysis is performed. The implementation is improved by

15 floor planning and trial layout generation which incorporates more or less accurate topological information, which is back-annotated into the standard delay format database. It finally concludes with the frozen layout. During this whole process the timing behavior concerning best case and worst case

20 (BC/WC) variations, load, wiring and/or routing estimations and/or variations can be characterized with the inventive delay chain preferably based on the dedicated boundary scan cells which elements are stable during the whole flow.

25 According to a second field of application, the delay measurement of fabricated devices may be performed. This can be done with a special but simple test-program on the production tester having a measurement feature.

30 Furthermore, the delay measurement can easily be done with the device mounted on board during a system-test and even in the field with the simple access and initialization possibilities as described above with regard to the IEEE

Standard 1149.1.

In all cases of preferred applications, the device quality, i.e. the location of the propagation delay within the BC/WC 5 (best/worst case) delay window can easily be determined.

Although the invention is described with regard to a preferred embodiment based on or derived from the IEEE Standard 1149.1, it should be obvious for a person skilled in 10 the art that several modifications depending on specific requirements can be carried out without departing from the protective scope of the invention.

Claims

1. Method for achieving delay measurement functionality of
5 an integrated circuit including the steps of
 - providing at least one boundary scan cell, each having a storage layer between a scan input port (SI) and a scan output port (SO) constructed to be used within a scan chain for boundary scan testability,
 - analyzing each scan cell to identify a redundant state
 - using this redundant state for creating an additional combinational path (BP) between the scan input port (SI) and a scan output port (SO) of a respective scan cell,
 - implementing each scan cell in the integrated circuit 15 by creating said scan chain.
2. Method of claim 1 wherein the step of providing comprises the providing of the at least one boundary scan cell according to the IEEE Standard 1149.1 or to a standard 20 derived from the IEEE Standard 1149.1.
3. Method of claim 1 or 2, wherein the step of creating an additional combinational path comprises the step of implementing a local path (BP) between said respective 25 two scan ports (SI, SO) by bypassing the respective storage layer of a boundary scan cell.
4. Method of claim 1, 2 or 3, wherein the combinational path is connected to the scan output port (SO) via a 30 multiplexer (MUX) controlled by the shift signal from a test access port controller.

5. Method of any of claims 1 to 4, comprising the step of connecting the scan input port (SI) of a first scan cell to a test data input port (TDI) for boundary scan testability and the scan output port (SO) of a scan cell forming the end of the scan chain via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan testability.
10. Method of any of claims 1 to 5, comprising the step of connecting the output port (SO) of a boundary scan cell forming the end of the scan chain to a separate delay chain output port (DCO).
15. Method of any of claims 1 to 6, wherein the combinational path (BP) is defined as false path during synthesizing of the scan chain.
20. A boundary scan cell including
 - an input port (PI) and an output port (PO) with a functional layer there between,
 - a scan input port (SI) and a scan output port (SO) with a storage layer there between, said storage layer is adapted to be used for achieving boundary scan testability,
 - a combinational path (BP) between the scan input port (SI) and the scan output port (SO) bypassing said storage layer.
25. Boundary scan cell of claim 8, wherein the scan cell is based on and conform to the IEEE Standard 1149.1 or a standard derived from the IEEE Standard 1149.1.

10. Boundary scan cell of any of claims 8 to 9, wherein the combinational bypass path (BP) and the storage layer is connected to the scan output port (SO) via a multiplexer (MUX) controlled by the shift signal from a test access port controller.

11. Boundary scan cell of any of claims 8 to 10, wherein the bypass path (BP) comprises at least one additional inverter, library and/or delay element (10).

10

12. Integrated circuit comprising a boundary scan chain having delay measurement functionality.

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13. Integrated circuit of claim 12, including at least one boundary scan cell according to any of claims 8 to 11, said scan cell is connected by means of said scan input and output ports (SI, SO) to form a scan chain, wherein the scan input port (SI) of a first scan cell is connected to a test data input port (TDI) and the scan output port (SO) of a scan cell forming the end of the scan chain is connected via a test data output path (BSR_TDO) to a test data output port (TDO) for boundary scan testability.

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14. Integrated circuit of claim 13, wherein the scan output port (SO) of the boundary scan cell forming the end of the scan chain is connected by means of said test data output path (BSR_TDO) to a separate delay chain output port (DCO).

30

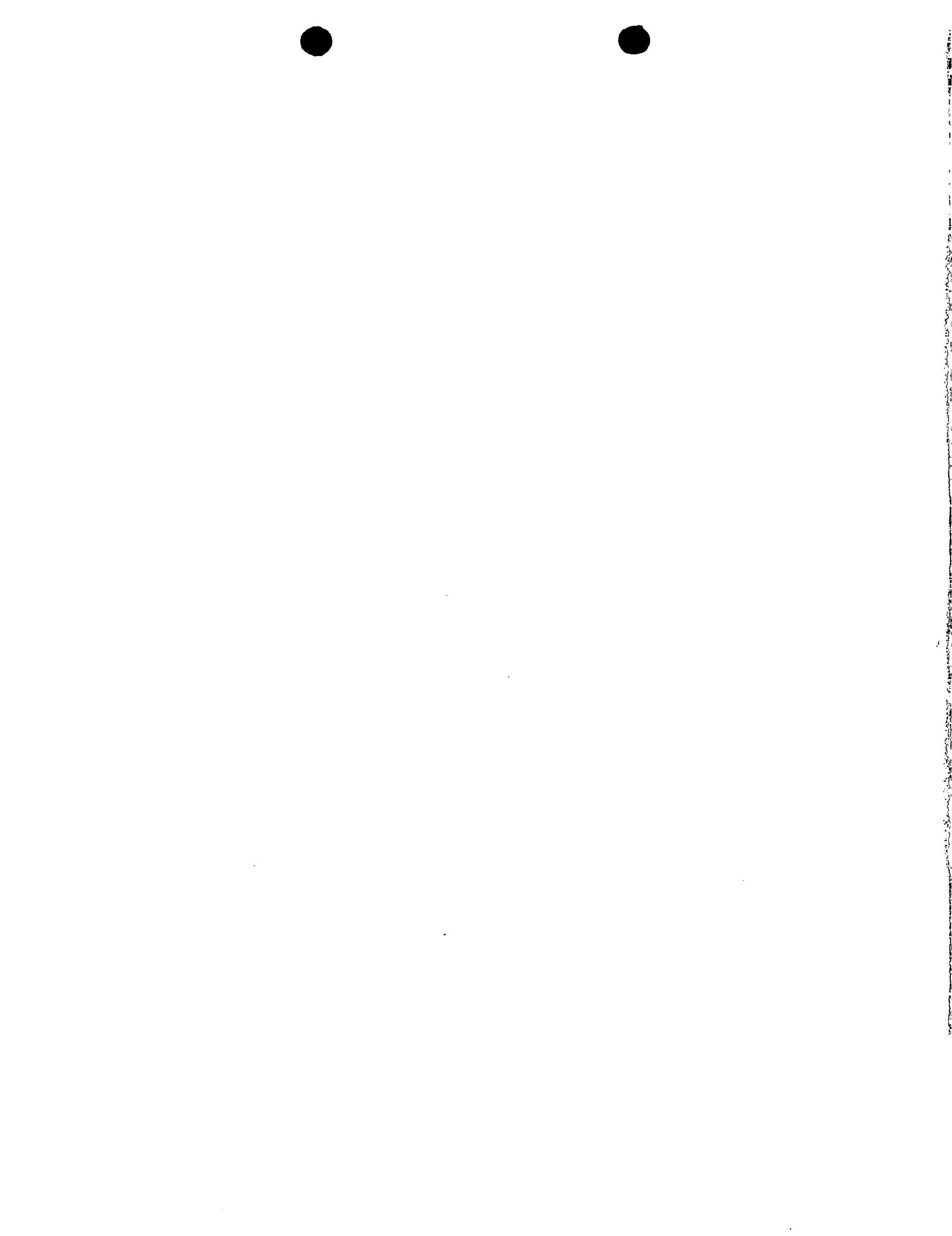
15. Integrated circuit of claim 14, wherein said test data output path (BSR_TDO) to the delay chain output pot (DCO)

is controllable by a test mode signal (TM).

16. Integrated circuit of claim 15, wherein said test mode signal (TM) is similar to a test pin for initializing other testability modes, in particular a RAM-test mode, a PLL test mode and/or a core scan test mode.
17. Electrical device comprising an Integrated circuit of any of claims 12 to 16.
18. Method for performing delay measurement of an integrated circuit of any of claims 12 to 16 or of a device of claim 17, including the steps of
 - entering a delay measurement mode,
 - applying of a test data signal on a test data input (TDI) for boundary scan testability,
 - performing the delay measurement at a port (TDO, DCO) connected to the test data output path (BSR_TDO) for scan testability.
19. Method of claim 18, wherein the step of entering comprises the step of entering a test-logic-reset-state.
20. Method of claim 18 or 19, comprising the step of performing the delay measurement at the test data output port (TDO) for boundary scan testability.
21. Method of claim 18 or 19, comprising the step of performing the delay measurement at a separate delay chain output port (DCO).

Abstract

The invention relates to the delay measurement functionality of integrated circuits. An object of the invention is to provide a new and improved approach for delay measurement of an integrated circuit that is substantially independent of vendors, technology and/or used development tools with a minimum of implementation effort in design time and gate resources. According to the invention, it is proposed to provide at least one boundary scan cell, each having a storage layer between a scan input port (SI) and a scan output port (SO) constructed to be used within a boundary scan chain of an integrated circuit for boundary scan testability, to analyze each boundary scan cell to identify a redundant state which is used to extend the boundary scan cell by creating an additional local path (BP) between the respective said scan input and scan output ports bypassing the respective storage layer and to implement the scan cell in the integrated circuit by creating said scan chain.



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Fig. 1

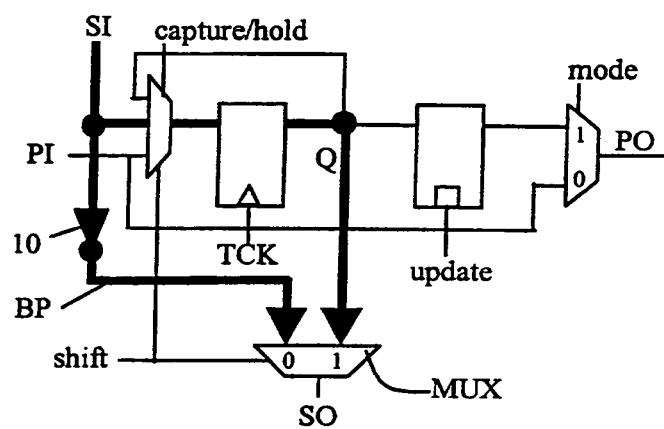
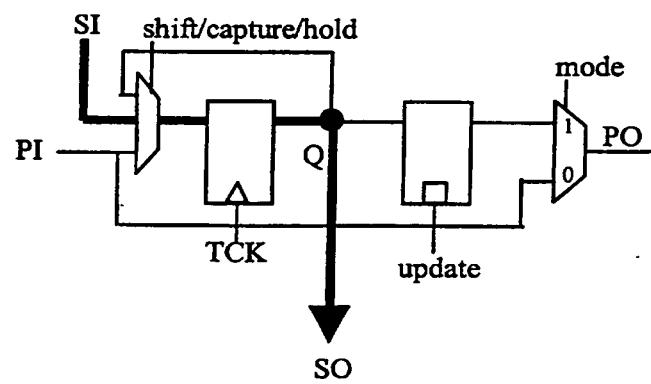


Fig. 2



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Fig. 3

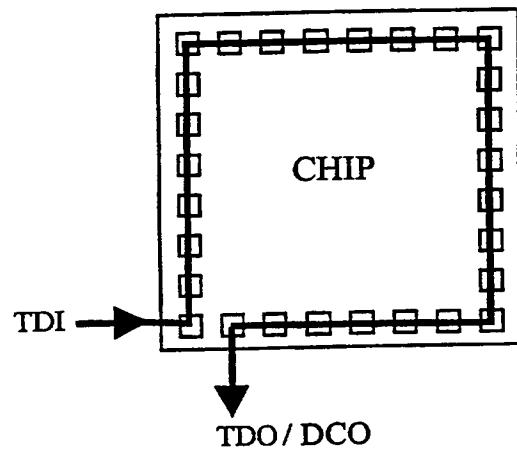


Fig. 4

